Roll No. .....

BCA–202(N)

B. C. A. (Second Semester) EXAMINATION, May, 2012

(New Course)

Paper Second

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION

Time : Three Hours] [*Maximum Marks : 75*

Note : Section A is compulsory. Attempt *seven* questions out of ten questions from Section B and *one* question from Section C.

Section – A

1. Choose the most appropriate answer. 1 each

(i) ..... decodes operation code of instruction.

(a) Multiplexer (b) Decoder

(c) Encoder (d) Demultiplexer

(ii) ..... is a binary coded hexadecimal equivalent of $(01100110)_2$.

(a) 66 (b) 77

(c) 44 (d) 99

P. T. O.

(iii) CPU processes instruction which resides in :

(a) Program Counter

(b) Instruction Register

(c) Address Register

(d) Index Register

(iv) ..... memory gives illusion of large memory.

(a) Associative (b) Set-associative

(c) Segmented (d) Virtual

(v) ..... is a storage device that stores information in such a manner that item stored first is retrieved first.

(a) Magnetic Disk (b) RAM

(c) Pen Derive (d) Magnetic Tape

(vi) Which one of the following is stated by De Morgan's theorem ?

(a) $y + 0 = y$ (b) $y \times 0 = 0$

(c) $y + 1 = y$ (d) $(y + z)' = y' \times z'$

(vii) In memory hierarchy, which of the following is the fastest memory ?

(a) Magnetic Disk (b) RAM

(c) Cache (d) ROM

(viii) Adjacent minterms in K-maps differ by :

(a) 1-bit

(b) 2-bits

(c) As many bits as the no. of variables

(d) None of these

2. (a) Simplify the Boolean function f using K-map in sum of product form. Draw the logic map with NAND gates : 7

$$F(w, x, y, z) = \Sigma (0, 1, 2, 4, 5, 6, 8, 12)$$

(b) Verify using Boolean Algebra : 3

$$(X + Y)(X + Z) = X + YZ$$

Section – B

3. Differentiate between the following : 6

(a) State table and excitation table

(b) Sequential and Combinational circuit

4. Construct a T flip-flop using : 6

(a) D-flip-flop

(b) JK flip-flop

Use blook diagram.

5. What is Multiplexer ? Construct a 16 : to – 1 line multiplexer with two 8 to – 1 and one 2 – to – 1 line multiplexer. Also write its truth table. 6

6. Design the basic gates by using NOR gate. 6

7. Discuss the memory hierarchy. Explain why this structure is used in computer ? How is the performance of memory system improved by using cache ? 6

8. (a) How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes ? 3

(b) How many lines of the address bus must be used to access 2048 bytes of memory ? How many of these lines with be common to all chips ? 3

9. Implement the full adder circuit with a decoder and two OR gate. Draw the truth table. 6

10. Obtain the simplified expression in sum of product for the following Boolean functions : 6

    (a) $F(x, y, z) = \Sigma(2, 3, 6, 7)$

    (b) $F(A, B, C, D) = \Sigma(7, 13, 14, 15)$

11. Design a BCD to decimal decoder. 6

12. Perform arithmetic operations : 6

    (i) $(-7)_{10} + (21)_{10}$ using two's complement

    (ii) $(-625)_{10} + (731)_{10}$ using ten's complement.

Section – C

13. (a) Design a synchronous BCD counter with JK flip-flops. 10

    (b) What is a Register ? Draw a block diagram of 4-bit register. 5

14. Write short notes on any *three* of the following : 5 each

    (i) Master slave flip-flop

    (ii) Virtual memory

    (iii) Associative memory

    (iv) Floating point representation

    (v) SRAM and DRAM memory organizations